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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,166	ZHANG, JIAN	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *3,4,12,16-18,25,29,30 and 34-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-11,13-15,19-24,26-28,31-33 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 10/4/2004 has been reviewed.

2. The amendment filed on 10/4/2004 has been entered (including amended claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 19, 20, 21, 22, 23, 24, 26, 27, 28; cancelled claims 3-4, 12, 16-18, 25, 29-30, 34-36 and a new claim 37).

3. Applicant's arguments filed on 10/4/2004 have been fully considered but they are not deemed to be persuasive.

4. The applicant contends, " Lahmeyer does not disclose decoding a portion of a first Reed-Solomon code word and no other portion of the first code word while storing a portion of a second Reed-Solomon code word, where the portion of the first code word is less than the entire first code word. That is, Lahmeyer decodes an entire Reed-Solomon code word in a period, no portions of a Reed-Solomon code word in respective multiple periods.

The examiner disagrees and asserts that Lahmeyer does not limit his invention to the code words. Lahmeyer also teaches that the data received is encoded in a Reed-Solomon code consisting of codewords made up of K data and N-K check symbols, where N is an arbitrary number and K is a number smaller than N (col. 2, lines 7-10, Lahmeyer). Lahmeyer teaches that although particular embodiments of the invention have been described and illustrated herein, it is recognized that modifications and variations may readily occur to those skilled in the art (col. 11, lines 22-25, Lahmeyer).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 5, 19, 20, 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Lahmeyer (US 4,649,541).

Lahmeyer anticipates claim 1.

Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit operable to: store a portion of a first Reed-Solomon code word, the portion being less than the entire first code word; store a portion of a second Reed-Solomon code word, the portion being less than the entire second code word; and while storing the portion of the second code word, decoding the portion of the first code word and no other portion of the first code word (col. 1, lines 12-15, lines 38-41, lines 51-54 and lines 59-65, col. 2, lines 7-10, Lahmeyer).

- Lahmeyer anticipates claim 5.

Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit operable to: receive m portions of a first Reed-Solomon code word, m being greater than one; receive m portions of a second Reed-Solomon code word after receiving the first code word; while receiving a first portion of the second code word, decoding a first portion of the first code word and no other portion of the first code word; and while receiving a second portion of the second code word, decoding the second portion of the first code word and no other portion of the first code word (col. 1, lines 12-15, lines 38-41, lines 51-54 and lines 59-65, col. 2, lines 7-10, Lahmeyer).

- Lahmeyer anticipates claim 19.

Lahmeyer teaches a method of operating a computing system with a Reed-Solomon decoding application comprising the steps of: receiving a portion of a first Reed-Solomon code word, the portion being less than the whole first code word; receiving a portion of a second Reed-Solomon code word, the portion being less than the whole second code word; and while receiving the portion of the second code word, decoding the portion of the first code word and no other portion of the first code word (col. 1, lines 12-15, lines 38-41, lines 51-54 and lines 59-65, col. 2, lines 7-10, Lahmeyer).

- Lahmeyer anticipates claim 20.

Lahmeyer teaches the method wherein the portion of the first Reed-Solomon code word is the same length as the portion of the second Reed-Solomon code word (col. 2, lines 7-10, Lahmeyer).

- Lahmeyer anticipates claim 23.

Lahmeyer teaches a method of operating a computing system with a Reed-Solomon decoding application comprising the steps of: receiving m portions of a first Reed-Solomon code word, m being greater than one; receiving m portions of a second Reed-Solomon code word after receiving the first code word and while receiving a first portion of the second code word, decoding a first portion of the first code word and no other portion of first code word; and while receiving a second portion of the second code word, decoding the second portion of the first code word and no other portion of the first code word (col. 1, lines 12-15, lines 38-41, lines 51-54 and lines 59-65, col. 2, lines 7-10, Lahmeyer).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2, 6, 7, 21, 22, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) in view of Deodhar (US 4,567,594).

As per claim 2, Lahmeyer substantially teaches the claim 1 (as rejected above).

However Lahmeyer does not explicitly teach the specific use of the computing system wherein: storing the portions of the first and second Reed-Solomon code words comprises storing each of the portions in a respective time having a duration t; and decoding the portion of the first code word comprises decoding the portion in the duration t.

Deodhar in an analogous art teaches that the above objects are accomplished in a preferred embodiment of the invention, which divides the Reed-Solomon decoding process into a sequence of well defined steps requiring a minimum of inter-step parameter transfers. These steps are implemented in the preferred embodiment by a plurality of processors, one for each of the defined steps, operating in a pipelined manner so as to provide efficient and fast decoding (figure 5, col. 2, lines 8-15, Deodhar). Deodhar teaches that the code words of a sector read from the disk are decoded over a plurality of consecutive time periods ...fourth and fifth time periods (col. 16, lines 20-49, Deodhar). Deodhar also teaches that a first processor ... the code words of the corresponding sector (col. 17, lines 46-57, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of using the computing system wherein: storing the portions of the first and second Reed-Solomon code words comprises storing each of the portions in a respective time having a duration t; and decoding the portion of the first code word comprises decoding the portion in the duration t.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce time delay for decoding the code words and the processing load on the decoder is evenly distributed at all times.

- As per claim 6, Lahmeyer and Deodhar teach the additional limitations.

Lahmeyer teaches the computing system and the processor circuit (col. 1, lines 38-41, Lahmeyer).

Deodhar teaches to receive the first and second portions of the second code word during respective first and second time periods each having a same duration and decode the first and second portions of the first code word during the first and second time periods respectively (col. 16, lines 61-68, col. 17, lines 1-14, lines 40-57, col. 18, lines 1-14, Deodhar).

- As per claim 7, Lahmeyer and Deodhar teach the additional limitations.

Lahmeyer teaches the computing system and the processor circuit (col. 1, lines 38-41, Lahmeyer). Deodhar teaches to receive m portions of a third Reed-Solomon code word; while receiving a first portion of the third code word, decoding a first portion of the second code and no other portion of the second code word; and while receiving a second portion of the third code word, decoding the second portion of the second code word and no other portion of the second code word (col. 16, lines 61-68, col. 17, lines 1-14, lines 40-57, col. 18, lines 1-14, Deodhar).

- As per claim 21, Lahmeyer and Deodhar teach the additional limitations.

Deodhar teaches the method wherein: receiving the portion of the second code word comprises receiving the portion of the second code word in a time T; and decoding the portion of the first code word comprises decoding the portion of the first code word in the time T (figure 5, col. 2, lines 8-15, col. 16, lines 20-49, col. 17, lines 46-57, Deodhar).

- As per claim 22, Lahmeyer and Deodhar teach the additional limitations.

Deodhar teaches the method wherein: the first and second code words each comprises m portions of equal-length (col. 5, lines 41-47, Deodhar).

- As per claim 24, Lahmeyer and Deodhar teach the additional limitations.

Deodhar teaches the method wherein: receiving the m portions of the first and second code words comprises receiving each of the m portions during a respective period of time T and decoding each of the first and second portions of the first code word during the same respective periods that the first and second portions of the second code word are received (col. 16, lines 61-68, col. 17, lines 1-14, lines 40-57, col. 18, lines 1-14, Deodhar).

10. Claims 8, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 5 and 23 above, and further in view of Oisel et al. (US 4,566,105).

As per claim 8, Lahmeyer substantially teaches the claim 5 (as rejected above). Lahmeyer also teaches the computing system wherein: the first and second Reed-Solomon code words each comprise n symbols (col. 2, lines 7-10, Lahmeyer).

However Lahmeyer does not explicitly teach specifically that n/m equals an integer that is greater than one.

Oisel et al. in an analogous art teach that N / M is a positive integer greater than one (col. 27, lines 5-6, Oisel et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Oisel et al. by including additionally that N / M is a positive integer greater than one.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using N / M, a positive integer greater than one would provide the opportunity to process the portions of the code word by different processors to reduce decoding time.

- As per claim 26, Lahmeyer and Oisel et al. teach the additional limitations.

Lahmeyer teaches the method wherein: the first and second code words each comprise n symbols (col. 2, lines 7-10, Lahmeyer).

Oisel et al. teach that n/m equals an integer greater than one (col. 27, lines 5-6, Oisel et al.).

11. Claims 9, 27, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) in view of Oisel et al. (US 4,566,105) and Deodhar (US 4,567,594).

As per claim 9, Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit (col. 1, lines 12-15, lines 38-41, Lahmeyer).

Lahmeyer teaches receiving m portions of each of Reed-Solomon code words, each code word comprising n symbols (col. 2, lines 7-10, Lahmeyer), while receiving a first portion of the second code word, decoding a first portion of the first code word according to a first algorithm and decoding no other portion of the first code word (col. 1, lines 51-54, lines 59-65, Lahmeyer).

However Lahmeyer does not explicitly teach that n/m equals an integer that is greater than one.

Oisel et al. in an analogous art teach that N / M is a positive integer greater than one (col. 27, lines 5-6, Oisel et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Oisel et al. by including additionally that n/m equals an integer that is greater than one.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using n/m equal to an integer that is greater than one would provide the opportunity to process the portions of the code word by different processors to reduce decoding time.

Lahmeyer also does not explicitly teach to receive five Reed-Solomon code words during respective time periods each having a duration; while receiving a first portion of the third code word, decoding a first portion of the second code word according to the first algorithm, decoding the first portion of the first code word according to a second algorithm, and decoding no other portions of the first and second code words; while receiving a first portion of the fourth code word, decoding a first portion of the third code word according to the first algorithm, decoding the first portion of the second code word according to the second algorithm, decoding the first portion of the first code word according to a third algorithm, and decoding no other portions of the first, second, and third code words and while receiving a first portion of the fifth code word, decoding a first portion of the fourth code word according to the first algorithm, decoding the first portion of the third code word according to the second algorithm, decoding the first portion of the second code word according to the third algorithm, decoding the first portion of the first code word according to a fourth algorithm, and decoding no other portions of the first, second, third, and fourth code words.

However Deodhar in an analogous art teaches a disk having data recorded in a track, said track being divided into a plurality of sectors, said data being recorded in each sector as a plurality of interleaved code words along with check data having values determined in accordance with Reed-Solomon decoding principles; means for sequentially reading sectors of data from said disk; and processing means to which sectors of data read from said disk are sequentially applied, said processing means being operative to detect and correct errors in sectors of data read from said disk by performing a plurality of consecutive processing operations thereon in accordance with said Reed-Solomon decoding principles; said

processing means comprising a plurality of processors, one for each of said consecutive processing operations, said processors operating in a pipelined manner and at a rate with respect to sequentially read sectors so as to provide for essentially real-time correction of data errors in sectors read from said disk (col. 16, lines 61-68, col. 17, lines 1-14, Deodhar).

Deodhar also teaches the invention, wherein said processing means operates over successive time periods, wherein said processing means includes a buffer for temporarily storing sectors of data applied to said processing means, and wherein said plurality of processors includes:

a first processor operative during each time period for receiving a new sector of data read from said disk and responsive thereto for producing partial syndrome signals representative of the partial syndromes of all of the code words of the corresponding sector;

a second processor operative during each time period and responsive to partial syndrome signals produced by said first processor one time period earlier for producing error location polynomial signals representative of the error location polynomial of the code words of the corresponding sector;

a third processor operative during each time period and responsive to error location polynomial signals produced by said second processor one time period earlier for producing error location signals representative of the locations of data errors in at least one of the code words of the corresponding sector;

said third processor also being operative during each time period in response to error location signals produced by said second processor two time periods earlier for producing error location signals corresponding to the locations of data errors for those code words of the corresponding sector for which error location signals were not produced by said third processor in the preceding time period (col. 17, lines 40-57, col. 18, lines 1-14, Deodhar).

Deodhar teaches a fourth processor operative during each time period and responsive to error location signals produced by said third processor one time period earlier for producing error value signals representative of the error values in at least one of the code words of the corresponding sector; said fourth processor also being operative during each time period in response to error location signals produced by said third processor two time periods earlier for producing error value signals representative

of code words of the corresponding sector for which error value signals were not produced by said fourth processor in the preceding time period; and

a fifth processor operative during each time period for receiving a different sector of data from said buffer and for correcting errors in the code words of a different sector in response to corresponding error location signals and error value signals produced by said third and fourth processors during previous time periods (col. 18, lines 15-35, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of receiving five Reed-Solomon code words during respective time periods each having a duration; while receiving a first portion of the third code word, decoding a first portion of the second code word according to the first algorithm, decoding the first portion of the first code word according to a second algorithm, and decoding no other portions of the first and second code words; while receiving a first portion of the fourth code word, decoding a first portion of the third code word according to the first algorithm, decoding the first portion of the second code word according to the second algorithm, decoding the first portion of the first code word according to a third algorithm, and decoding no other portions of the first, second, and third code words and while receiving a first portion of the fifth code word, decoding a first portion of the fourth code word according to the first algorithm, decoding the first portion of the third code word according to the second algorithm, decoding the first portion of the second code word according to the third algorithm, decoding the first portion of the first code word according to a fourth algorithm, and decoding no other portions of the first, second, third, and fourth code words.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to spread the decoding processing load on the processors evenly by decoding one portion of a code word while receiving the next portion of a code word and minimize system failure.

- As per claim 27, Lahmeyer, Oisel et al. and Deodhar teach the additional limitations.

Lahmeyer teaches a method of operating a computing system with a Reed-Solomon decoding application (col. 1, lines 12-15, lines 38-41, Lahmeyer). Lahmeyer teaches receiving m portions of each of Reed-

Solomon code words, each code word comprising n symbols (col. 2, lines 7-10, Lahmeyer), while receiving a first portion of the second code word, decoding a first portion of the first code word according to a first algorithm and decoding no other portion of the first code word (col. 1, lines 51-54, lines 59-65, Lahmeyer).

Oisel et al. teach that n/m equals an integer that is greater than one (col. 27, lines 5-6, Oisel et al.).

Deodhar teaches receiving five Reed-Solomon code words during respective time periods each having a duration; while receiving a first portion of the third code word, decoding a first portion of the second code word according to the first algorithm, decoding the first portion of the first code word according to a second algorithm, and decoding no other portions of the first and second code words; while receiving a first portion of the fourth code word, decoding a first portion of the third code word according to the first algorithm, decoding the first portion of the second code word according to the second algorithm, decoding the first portion of the first code word according to a third algorithm, and decoding no other portions of the first, second, and third code words and while receiving a first portion of the fifth code word, decoding a first portion of the fourth code word according to the first algorithm, decoding the first portion of the third code word according to the second algorithm, decoding the first portion of the second code word according to the third algorithm, decoding the first portion of the first code word according to a fourth algorithm, and decoding no other portions of the first, second, third, and fourth code words (col. 16, lines 61-68, col. 17, lines 1-14, col. 17, lines 40-57, col. 18, lines 1-14, lines 15-35, Deodhar).

- As per claim 37, Lahmeyer, Oisel et al. and Deodhar teach the additional limitations.

Lahmeyer teaches the method wherein the portions of the five Reed-Solomon code words each have a same size (col. 2, lines 7-10, Lahmeyer).

12. Claims 10-11, 14, 28, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) in view of Oisel et al. (US 4,566,105).

As per claim 10, Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit (col. 1, lines 12-15, lines 38-41, Lahmeyer) operable to: sequentially receive m portions of the Reed-Solomon-encoded string of data in T seconds, the string of data including n symbols; sequentially calculate m respective partial syndromes for the m

portions of the string, the processor circuit operable to calculate each of the m partial syndromes in T/m seconds; from the m partial syndromes, sequentially calculate the coefficients of m respective sets of error locator polynomials, the processor circuit operable to calculate each set of coefficients in T/m seconds; sequentially determine m respective sets of roots for the sets of the error locator polynomials, the processor circuit operable to determine each set of roots in T/m seconds; for each of the m sets of roots; sequentially determine the magnitude of respective error in T/m seconds; and sequentially correct each of the errors in T/m seconds (col. 2, lines 3-37, Lahmeyer).

However Lahmeyer does not explicitly teach the specific use of n/m equaling a first integer that is greater than one.

Oisel et al. in an analogous art teach that N / M is a positive integer greater than one (col. 27, lines 5-6, Oisel et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Oisel et al. by including additionally n/m equaling a first integer that is greater than one.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using n/m equaling a first integer that is greater than one would provide the opportunity to process the portions of the code word by different processors to reduce decoding time.

- As per claim 11, Lahmeyer and Oisel et al. teach the additional limitations.

Lahmeyer teaches the computing system wherein: the n symbols each comprises b bits, k of said n symbols comprise data symbols; n-k of said symbols comprise parity symbols (col. 2, lines 7-11, Lahmeyer).

Oisel et al. teach that (n-k)/m equals a second integer; and k/m equals a third integer (col. 27, lines 5-6, Oisel et al.).

- As per claim 14, Lahmeyer and Oisel et al. teach the additional limitations.

Lahmeyer teaches the computing system wherein the processor circuit executes a Chien Search to determine the roots of the error locator polynomial (col. 8, lines 3-5, Lahmeyer).

- As per claim 28, Lahmeyer and Oisel et al. teach the additional limitations.

Lahmeyer teaches a method of operating a computing system with a Reed-Solomon decoding application (col. 1, lines 12-15, lines 38-41, Lahmeyer) comprising the steps: sequentially receiving m portions of the Reed-Solomon-encoded string of data in T seconds, the string of data including n symbols; sequentially calculate m respective partial syndromes for the m portions of the string, the processor circuit operable to calculate each of the m partial syndromes in T/m seconds; from the m partial syndromes, sequentially calculate the coefficients of m respective sets of error locator polynomials, the processor circuit operable to calculate each set of coefficients in T/m seconds; sequentially determine m respective sets of roots for the sets of the error locator polynomials, the processor circuit operable to determine each set of roots in T/m seconds; for each of the m sets of roots; sequentially determine the magnitude of respective error in T/m seconds; and sequentially correct each of the errors in T/m seconds (col. 2, lines 3-37, Lahmeyer). Oisel et al. teach n/m equaling a first integer that is greater than one (col. 27, lines 5-6, Oisel et al.).

- As per claim 32, Lahmeyer and Oisel et al. teach the additional limitations.

Lahmeyer teaches the method wherein the processor circuit executes a Chien Search to determine the roots of the error locator polynomial (col. 8, lines 3-5, Lahmeyer).

13. Claims 13, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) and Oisel et al. (US 4,566,105) as applied to claim 10 above, and further in view of Oh et al. (US 5,583,499).

As per claim 13, Lahmeyer and Oisel et al. substantially teach the claimed invention described in claim 10 (as rejected above).

However Lahmeyer and Oisel et al. do not explicitly teach the specific use of the computing system wherein the processor circuit executes a Berlekamp-Massey Algorithm to calculate the coefficients of the error locator polynomial.

Oh et al. in an analogous art teach that a popular algorithm for obtaining the coefficients of the error locator polynomial is the Berlekamp-Massey algorithm (col. 2, lines 8-10, Oh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Oh et al. by including an additional step of using

the computing system wherein the processor circuit executes a Berlekamp-Massey Algorithm to calculate the coefficients of the error locator polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide apparatus for implementing Galois field arithmetic using fewer components, fewer data paths and higher speed than a general purpose digital computer employed for this purpose.

- As per claim 31, Lahmeyer, Oisel et al. and Oh et al. teach the additional limitations.

Oh et al. teach the method wherein the computing system executes a Berlekamp-Massey Algorithm to calculate the coefficients of the error locator polynomial (col. 2, lines 8-10, Oh et al.).

14. Claims 15, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) and Oisel et al. (US 4,566,105) as applied to claim 10 and 28 above, and further in view of Sammartino et al. (US 6,511,280 B1).

As per claim 15, Lahmeyer and Oisel et al. substantially teach the claimed invention described in claim 10 (as rejected above).

However Lahmeyer and Oisel et al. do not explicitly teach the specific use of the computing system wherein the processor circuit executes a Forney Algorithm to determine the magnitude of the errors in the received digital code word.

Sammartino et al. in an analogous art teach finding the roots of the ti(x) to determine the error locations, and determining the magnitude of the errors and erasures by applying a modified version of the Forney algorithm (col. 6, lines 37-40, Sammartino et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Sammartino et al. by including an additional step of using the computing system wherein the processor circuit executes a Forney Algorithm to determine the magnitude of the errors in the received digital code word.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to use concatenated coding for implementing a code with a very long block length and a large error-correcting capability.

- As per claim 33, Lahmeyer, Oisel et al. and Sammartino et al. teach the additional limitations. Sammartino et al. teach the method wherein the processor circuit executes a Forney Algorithm to determine the magnitude of the errors in the received digital code word (col. 6, lines 37-40, Sammartino et al.).

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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